PC "Baltika"

Author Unknown (Hardcover lost booklet).
Revised rimf (rimf@inbox.ru).

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Content

1. Introduction

At the end of the 1980s in the Soviet Union, widespread personal computers (PCs), self-production, which, in one way or another is repeated one of the most common PC ZX Spectrum British company Sinclair Research. This book is considered a PC "Baltika", as one of the most common, contrasting combines minimum cost of components and maximum possible gaming options.

The purpose of this paper is to briefly convey information about the appointment of the circuit elements, the intricacies of installation, recommendations for the launch of an electronic computer and completions, by which you will be able to eliminate the defects that arise in the game programs.

Before considering a specific scheme, consider the general characteristics and principles of the ZX Spectrum computers and "Baltika".

1.1 Brief specifications

- used CPU Zilog Z80A CPU (or MME UA880D PC "Baltika")
- clock frequency of 4 MHz (3.5 MHz in the ZX Spectrum)
- KiB RAM volume 64 (48 KiB in ZX Spectrum)
- ROM 16 KiB volume
- resident software Basic / Monitor software

Features supported by the screen

- as the monitor is used household TV
- resolution graphics mode - 256 * 192
- number rows - 24
- the number of characters per line - 32
- Palette - 8 Colors
- halftone screen, 2 shades of gray, flicker mode keyboard Features
- matrix, 40 keys
- 5 registers

CPU

As the central processing element used in the ZX Spectrum common eight-bit microprocessor Z80 company Zilog. Consider the appointment of its conclusions:

D0-D7 data bus. 8 bidirectional tri-state is used for input-
Output data of the microprocessor, memory and peripherals.

A0-A15 address bus. 16 lines with three states, is used to address 65536 yacheek memory 65536 and input-output ports. The ZX Spectrum may appeal only to the 32,768 odd addresses IO, as at zero at A0, due to incomplete address decoding is always input-output port 254 (#FE) is chosen, which is involved in the ZX Spectrum under operation with a tape recorder, the audio output, the output of border colors and keyboard polling. When addressing ports water / output increasingly using A0-A7 lines, i.e. 256 addresses. Note that in this case on lines A8-A15 the contents of register B is present microprocessor.

2

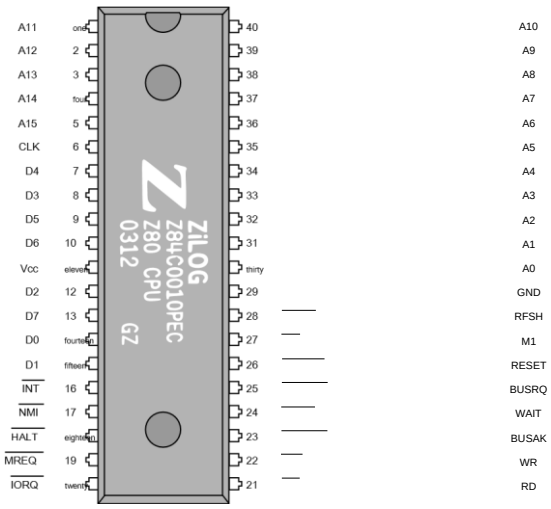


Fig. 1: The microprocessor Zilog Z80 with the names of the conclusions

/ M1 Automatic cycle 1. The output signal, active low indicates that the MP fetches from memory the next operation code, together with the signal / IORQ serves to interrupt acknowledge.

/ MREQ Query memory. The output signal of tri-state active low level indicated It binds to use the memory address space, rather than input-output.

/ IORQ IO request. Similar / MREQ signal, but it indicates the use LocationNogo IO space rather than memory.

/ RD Reading. The output tri-state, active low indicates that the memory of the MP performs a read operation or an input-output device.

/ WR Entry is the same as / RD, but for a write operation.

/ RFSH Regeneration. The output signal is active low indicates that the bus addresses A0 to A6 contains the address of the regeneration of dynamic memory that produces MP Z80 independently during decoding the opcode.

/ HALT Stop. The output signal of an active low indicates that the MP performs command and the program stops until the interrupt will perform the idle stop state team for memory recovery.

/ WAIT Waiting. Input active with a low level. Ispolzuetsyamedlennymi ustroystvami memory or input-output for translation MT in idle state, before they are ready for data transfer.

/ INT An interrupt request. The input signal is active-low. This interrupt can be disabled (masked) or authorized by the MP commands. The ZX Spectrum every 20 milliseconds the input / INT goes negative pulse generated by hardware on which MP proceeds to the keyboard service program, increments the clock, etc.

/ NMI NMI. signal decline at this input activates the internal trigger NMI, and automatically leads MP to make a restart (the restart) with address 102 (# 0066).

/ RESET Reset. Active low on this input resets the program counter, registers and I R, 0 sets the interrupt and resets the interrupt enable flip-flop mode, during the active signal / RESET address bus and data bus are in the third state, and all control signals are inactive.

/ BUSRQ request access to the bus. The input signal is active-low. MP completes current cycle, and then translates the address bus and data bus, as well as tristate output control signals in a high impedance state in order to give management of these tires other devices.

/ BUSACK Providing access to the bus. The output signal of the active low ukazyINDICATES THE MP handed over control tires to the requesting device.

CLK Isochronous. Entrance.

1.2 Address space ZX Spectrum

Z80 has a 16-bit address bus, so the maximum amount of memory that it can be addressed with no additional hardware is 64 kibibyte (KiB).

The ZX Spectrum memory is allocated as follows. Since addresses 0 to 16383 (# 0000... # 3FFF) is ROM area (or region ROM). This area is divided into 3 parts:

1. 7 kibibyte - OS (operating system); 2. 8

kibibyte - BASIC language interpreter;

3. 1 kibibyte - generator marks (symbols).

The rest of the memory from the address of 16384 through 65535 occupies an area of random access memory (or RAM area). In turn, the RAM is divided into areas that are used by the operating system and BASIC language interpreter.

Consider two memory areas are used for display on the TV screen information:

1. The area of the screen;
2. The region attributes.

screen area occupies addresses 16384 of 22527 (# 4000... # 57FF). There is one correspondence between the bits in the memory and the points on the TV screen. Screen ZX Spectrum comprises 256 horizontal dots and 192 vertical dots. Each displayed character is a matrix of dots 8 * 8 (familiarity). Thus screen 24 has the character string of 32 characters per line.

The following calculations show that the number of bits in the six kibibyte memory area of the screen is the number of points on the TV screen connected to the ZX Spectrum.

6 KiB = 1024 * 8 * 6 = 49152 bits 32 * 24 * 64 =
49152

1024 - the number of bytes in one kibibayte,

8 - the number of bits in one byte,

6 - kibibyte number of occupied area of the screen,

32 - the number of symbols (character cells) in a row,

24 - number of lines,

64 - the number of points in the matrix of familiarity.

the TV screen is divided into three parts: familiarity lines numbered 0-7 correspond to addresses of 18431 to 16384 (# 4000 # 477F...), lines 8-15 of addresses with 18432 20479 (# 4800 # 4FFF...), lines 16-23 20480 addresses by 22527 (# 5000... # 57FF).

Screen memory area includes information for displaying the corresponding screen pixels, and to determine their color region attribute is used.

ZX Spectrum screen has a 768 character cells, they are easy to calculate. Each familiarity on the TV screen corresponds to one byte attributes. Therefore, the region attribute occupies the volume of 768 bytes and is located in the addresses of 23295 to 22528 (# 5800... # 5AFF). Bits of the attribute byte are distributed as follows: Bits 0-2 determine the color of the ink (see Table 1..); Bits 3-5 determine the color of the paper (see Table 1..); bit 6

brightness (if bit 6 at zero, the symbol is displayed with reduced brightness, when in unit - then with increased).

bit 7 blink (when the bit 7 in the unit, the character that corresponds to the attribute will flash).

The ZX Spectrum image occupies not the entire TV screen, but only a part. Along the edges of the screen is the so-called curb (Border), border color is set programmatically and may have one of eight basic colors (see. Table. 1).

four

Table 1: Color Coding Color attribute bits 0

(3) 1 (4) 2 (5) 0			
	0	0	the black
one	0	0	blue
0	one	0	red
one	one	0	purple
0	0	one	green
one	0	one	blue
0	one	1	yellow
one	one	one	white

1.3 Keyboard

ZX Spectrum keyboard has 40 keys, so it is multifunctional. Each key can be interpreted in different ways, depending on the «K» cursor mode, «L», «E», «G», «C». Every 20 milliseconds, an interrupt signal / INT microprocessor produces keyboard polling.

2 Description concept

Before considering the circuit diagram (see. Fig. 2), we should say that in the PC "Baltic", unlike the other embodiments and corporate ZX Spectrum, microprocessor clock frequency of 4 MHz (3.5 MHz other embodiments).

2.1 Generator and frequency dividers

The crystal oscillator is assembled according to the classical scheme of two inverters D37.6 and D37.5. The pulses from the frequency of 16 MHz output from D37.4 (8) are fed to the counting inputs of the counters D20, D21, D22. Counters are assembled on the circuit with a parallel displacement between counters for IMSK555IE10. Transfer Signal from D22 (15) acts on the counting input D23.1 (1). Counters D20, D21, D22, D23.1, D23.2 used as frequency dividers, the signals from the outputs of these counters are used to synchronize the operation of the whole circuit.

Since D20 output (13) the pulses with a frequency of 4 MHz, D37.3 through inverter are input (6) D48 cell synchronizing operation of the microprocessor.

2.2 reset signal

Forming circuit reset signal (RESET, / RESET) is implemented on two inverters and D38.5 D38.4.

The reset signal is generated in the two cases:

1. Pressing the Reset button;
2. When you turn on the power.

At power on D48 (26) (input / RESET) would be zero during the time until the capacitor C2 is charged to a logic-one level. The duration of the active pulse of the reset signal depends on R3, C2 chain. VD1 diode is used for the rapid discharge of the capacitor C2 at the time of power failure. Furthermore reset signal D38.5 (10) is applied to D44 (35) (RES input) by adjusting all three ports of the parallel interface (application on p. 30) in the zero mode input.

From the output of D38.4 (8), the reset signal is supplied to D41 (1) setting all bits of this register to zero.

After the reset signal the microprocessor at address zero selects the first reset command subroutine disposed in ROM (D46, D47).

2.3 ROM

FIELD ROM (D46, D47) is implemented on a ROM type 2764 (an analogue K573RF4). Selection D46 or D47 is made, provided at the terminals 20 (/ CS) 22 and (/ OE) is present a logical zero. A logic zero on D46 (20), D47 (20) is present provided that the level A14 and A15 addresses are in the ground state and the microprocessor put on the bus signals / RD control and / MREQ, this state corresponds to a memory read cycle. Another condition is a ROM select Stock D33.2 (5) the zero signal level / ENROM, formed on D41 (10) (Rom off). This node is implemented on elements D33.2, D33.3, D37.1, D38.1. Selection of entry ROM / CS (D46 (22), D47 (22)) is performed using an address bit A13. ROM D47 is disposed in the lower region of ROM addresses and A13 is selected directly signal.

2.4 RAM

When handling the microprocessor to the RAM address bits A14 and A15, or at least one of them should be in a single state, in these conditions with D33.2 logic zero output (6) of the elements and D32.1 D32.2 and with a signal / DAT is supplied to D13 (19). At this signal D13 member, withdraw from their tires trohstabilnoe state, and the microprocessor can access the RAM. Direction of transmission depends on the signal / RD, input to the output D13 (1). At zero level / RD information is transferred from the RAM on the microprocessor data bus, single level - from the microprocessor to the RAM.

FIELD RAM memory chips implemented on K565RU5 (D1-D8), 64 KiB (D1-D8 capacity) is used only 48 KiB. The remaining 16K in ZX Spectrum mode are not used and programmatically inaccessible.

The address on the memory chip D1-D8 comes from two sources:

1 when accessing the memory of the microprocessor;

2. The address information supplied from the sampling circuits of the display area and the region attributes for display on the TV screen.

Address itself chips D1-D8 is adopted in two stages. At the signal / RAS (/ MRAS) - adopted by the lower eight address bits, and the signal CAS (/ MCAS) - the eight most significant bits of the address. Selection source high and the low half of the address is carried out by multiplexers D14, D15, D16, D17 using control signals and AP0 AP1 D26 (2, 3). Conclusions 2 and 4 at the D1-D8 elements are combined among themselves, since D1-D8 (14) has a data output state and trohstabilnoe during recording does not affect the D1-D8 inputs (2).

Synchronizing the memory access and memory formation control signals D26 next element. In more detail the formation of the control signals and synchronize memory accesses from various sources discussed below.

2.5 Addresses screen areas and attributes

Elements D18 and D9.1-D9.3 are designed to address the formation of the screen area and the attributes. Location attribute field generated at the zero signal / ABT D26 (4) is formed at a single level address of the screen area. These addresses through D14-D17 multiplexers fed to the RAM chip in which information is selected for display. D18 firmware ROM K155RE3 «D» refer to page 12.

2.6 Control signals

Consider the generation of control signals and memory timing. It uses ROM K155RE3 «M» (D26). Firmware of the ROM is shown on page 12, and the timing diagrams in Figure 4.

All eight control signals removed from D26 outputs have repetition period of 1 microsecond.

The timing chart (. Figure 4) consider the sixteenth cycle:

1. In the sixteenth cycle:
   (A) a signal / WAIT D26 (1) goes to logic one. With thissignal at terminal 24 D48 microprocessor, the microprocessor removes the idle state and moves to the next memory access cycle;
   (B) signals and AP0 AP1 D26 (3, 2) become the logic zero state. these signalssupplied to the address inputs of multiplexers D14-D17, which commute address on the address bus D1-D8 from different sources in accordance with Table 2.

Table 2: Switching address for the RAM chips AP0 AP1 Note 0

	0	On the address bus D1-D8 8 LSBs come from the microprocessor address.
0	one	On the address bus D1-D8 comes 8 LSBs of the address for fetching a byte from the screen area or region attributes for display.
one	0	On the address bus D1-D8 receives the upper 8 bits of the microprocessor address.
one	one	On the address bus D1-D8 receives the upper 8 address bits for selecting a byte from the screen area or region attributes for display.

2. In the first cycle:
   (A) the decay of the signal / RAS D26 (9) The eight LSBs of the address from the microprocessortaken into the internal register D1D8, signal / MRAS, arriving at a conclusion D1D8 (4) formed from the signal / RAS via D25.2 member (D25.2 used as delay);
   (B) AP0 signal transitions in one state and switches on the address inputs D1-D8 eight most significant bits of the address from the microprocessor;
   (C) signal / WRE D26 (6) goes to zero state, and with the proviso that the microprocessorperforms recording in the RAM (i.e., / WR = 0, / RD = 1, / RFSH = 1, / MREQ = 0 and A14 and A15 are not equal to zero - is a logical expression implemented on elements D33.1, D32.1 D31.2, D33.3, D37.2) at the terminals of the 3 D1-D8 will write signal (zero level). Otherwise be present read signal (high level). (D) low signal / DAT D26 (7) for circulation of the microprocessor in RAM otkryva-

   a bus driver D13. The transmission direction through the bus driver D13 will depend on the signal / RD D48 (21). / RD = 0 - RAM of the microprocessor data bus. / RD = 1 - from the microprocessor to the RAM.

3. In the second cycle:
   (A) by CAS D26 (5) signal which, via the elements supplied D25.3 D25.4 and the conclusions D1-D8 (15) accepted the upper 8 address bits, and in the same clock cycle there is a record in the RAM or reading from RAM.

4. In the third cycle signal is removed / WRE.
5. In the fourth clock cycle removed signal / RAS.
6. In the fifth time step:
   (A) a signal / WAIT D26 (1) goes to the zero state and MP, interrogating this conclusion, inthe beginning of the next cycle will enter into a state of "expectation" and will stay there until until the D48 input (24) is a high level appears.
   (B) AP0 = 0, and AP1 = 1. As a result, 8 LSBs attribute area address receivedon address inputs D1-D8.
7. In the sixth clock signal is removed CAS D26 (5).
8. In the seventh cycle:
   (A) the decay of the signal / RAS D26 (9) lower eight address bits are taken into intrarenny register D1-D8;
   (B) AP0 proceeds in one state giving significant bits of the address for the samplingfield attribute byte of D1-D8 on the address bus.

9. In the eighth cycle:

   (A) the older bits in the address are received by the inner edge of CAS D26 (5) of the signalregisters D1-D8;

   (B) passing the signal / DAT D26 (7) in one state closes the formation busVatel D13.

10. In the tenth cycle:

    (A) is removed CAS D26 signal (5);

    (B) on the edge of the signal / ABT D26 (4) bytes selected from the region attribute is adoptedto the register D11. Furthermore, when the unit level of signal / ABT, using D18 cells, D9.1, D9.2, D9.3 formed byte address of the screen area.

11. In the twelfth cycle along the front CAS D26 (5) can only MSBs of the screen area. LSB address area of the screen and the corresponding attribute byte field coincide, and therefore the lower address bits which have been taken into D1-D8 internal registers in the seventh clock, used for selecting data from the RAM. Such D1-D8 called page mode read / write mode.

12. In the fourteenth clock cycle reset signal / RAS D26 (9).

13. In the fifteenth clock cycle removed CAS D26 signal (5) and / ABT D26 (4). In the same stroke element D31.1 formed TT signal which is received in the register D12 bytes of RAM and a display area is rewritten contents of register to register D11 D10.

In the next cycle, there is a display of the two selected bytes are in the registers D10 and D12, and the sample next two bytes.

2.7 color signals for TV

Now consider how the generation of signals R, G, B of the bytes of the selected screen area (byte stored in the register D12) and area attributes (D10). In addition to these registers for generating chrominance signals are used three digits in which the register D42 shows information about a border color.

Explanation mnemonic signal designation registers D10 and D42 (see. Fig. 1) is shown below.

Mnemonics except FL and I is interpreted as follows. The first character corresponds to one of the three primary colors:

- R - red (Red)
- G - green (Green)
- B - blue (Blue)

The second character is interpreted as follows:

- I - color ink (Ink)
- P - color paper (Paper)
- B - Border color (Border)

I - a signal of high or low intensity (brightness).

FL - if the signal is in one state, the display will flash familiarity.
Each digit register D12 correspond to the point on the TV screen. If the discharge is cleared to zero, then the point is lighted color of the paper, and if set to one - the ink color. The contents of register bits D12 through D19 in the multiplexer is fed to a serial code D25.1 input (1). The second input of D25.1 (2), unless the flashing bit (FL), is fed logical unit. If FL is in the set condition, then D25.1 (2) receives pulses at a frequency of about 2 Hz, and the display flashes on the TV screen. Counters and D43.1 D43.2 divided frequency to the frequency with which the symbol is flashing displayed on the screen. Use of signal points illuminates D25.1 (3) and signals taken from the outputs of D27 (12), D27 (11) are formed and signals POINT BORD.

2.8 synchronizing signal TV

Signal SYN is formed by D27 and D28 cells. These ROM firmware are listed on page 12. A mixture of horizontal and vertical sync pulses SYN withdrawn D27 outlet (10).

2.9 Interrupts

Every 20 milliseconds the signal output from D28 (12) via a diode VD2 is supplied to the reset input of counters D23.1 (7), D23.2 (15) and the input D39.2 trigger (11), writing a logic zero into it. The output of flip-flop D39.2 (9) of the zero signal is input maskable interrupt of the microprocessor / INT D48 (16). In the cycle interrupt service routine the microprocessor proceeds to keyboard polling routine.

Resetting the flip-flop made zero signals / M1 D48 (27) and / IORQ D48 (20) through D32.4 element.

2.10 IO Ports

To address ports, I / O decoder IC used K555ID4 (D34). Information about the border color is output to the register D42 (19, 16, 15). Also in this register is output audio signal D42 (2) and information for a tape recording D42 (5). On D44 item sold three ports.

Port A - typically used to connect a joystick, ports B and C, the user can use at their discretion (to connect the printer, etc.).

Keyboard port and an input port for reading from the tape carried on the elements of IC K561LN1 (D35).

Port implemented in the D41, allows the user to select one of four screen space. Selection Display is performed using two bits D41 (2, 7). Standard monitor ZX Spectrum uses only one screen space, which begins with the address # 4000, in addition to this port outputs the signal / ENROM to enable (disable) the ROM D41 (10).

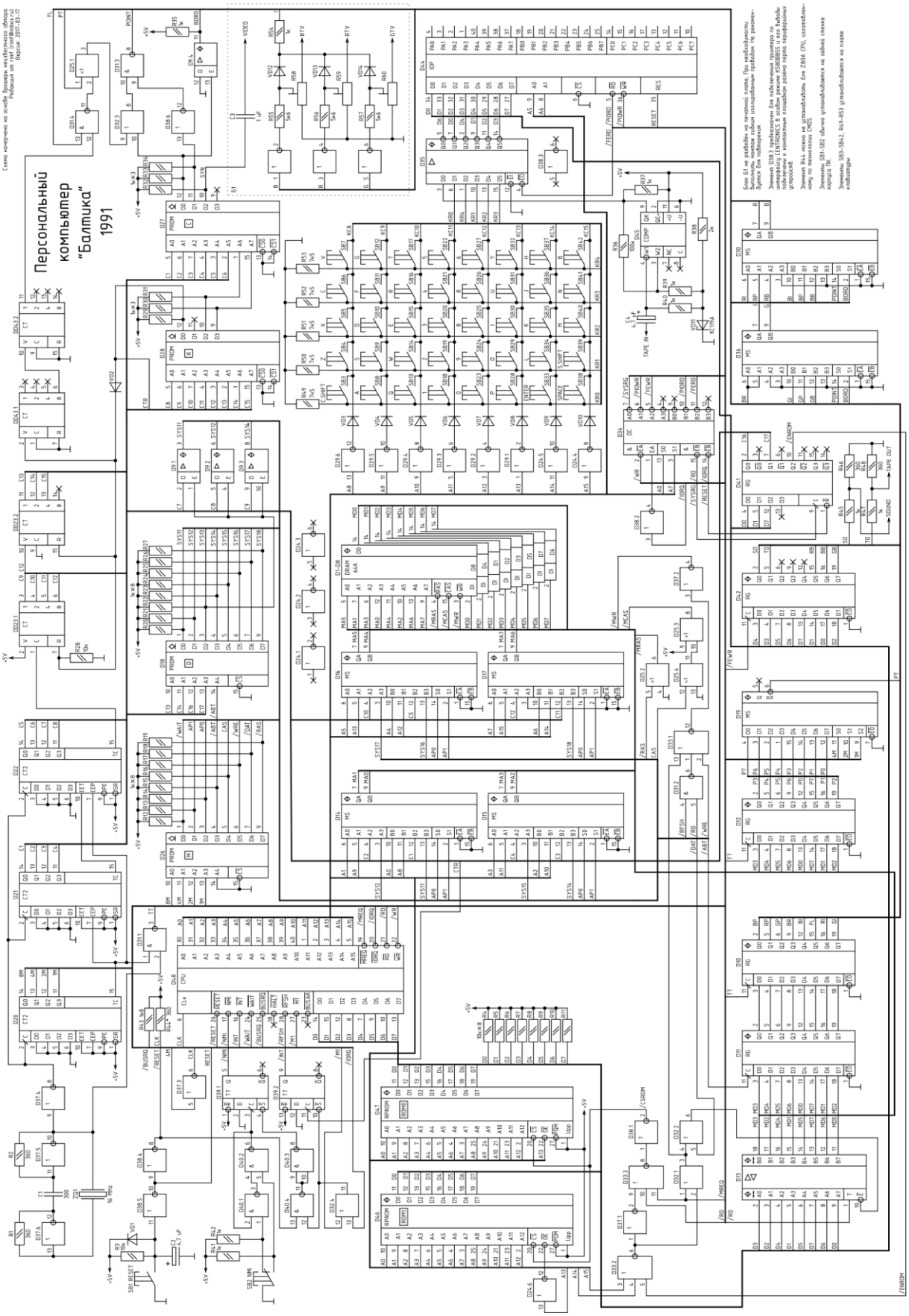


Fig. 2: Schematic diagram of the PC "Baltika"

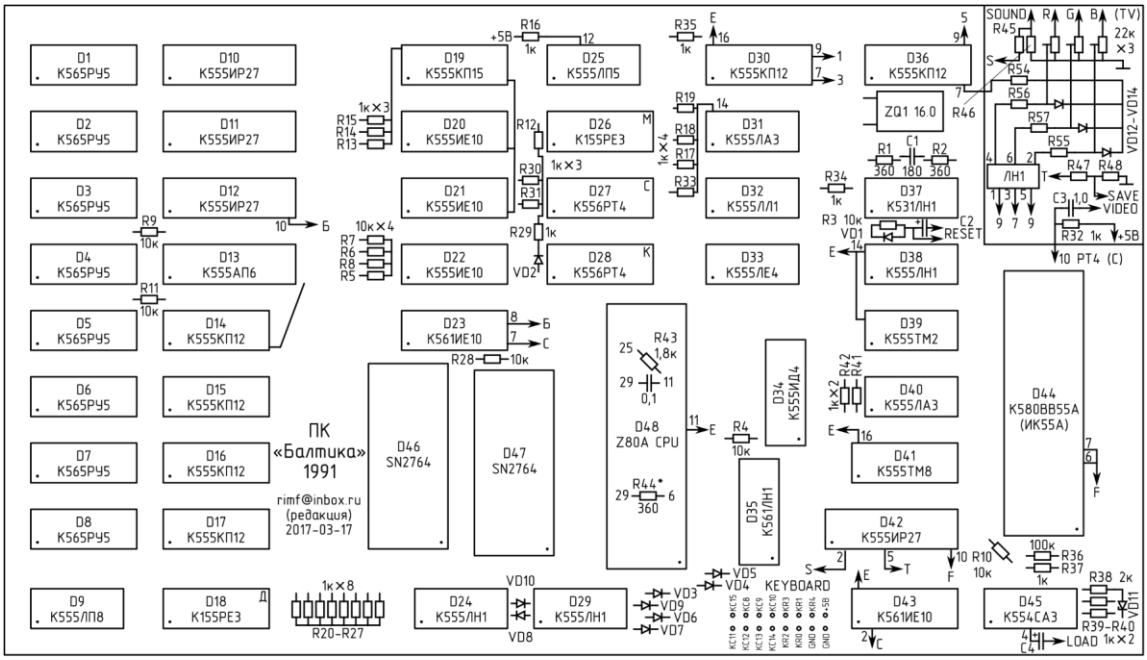


Fig. 3: Wiring diagram PC "Baltika"

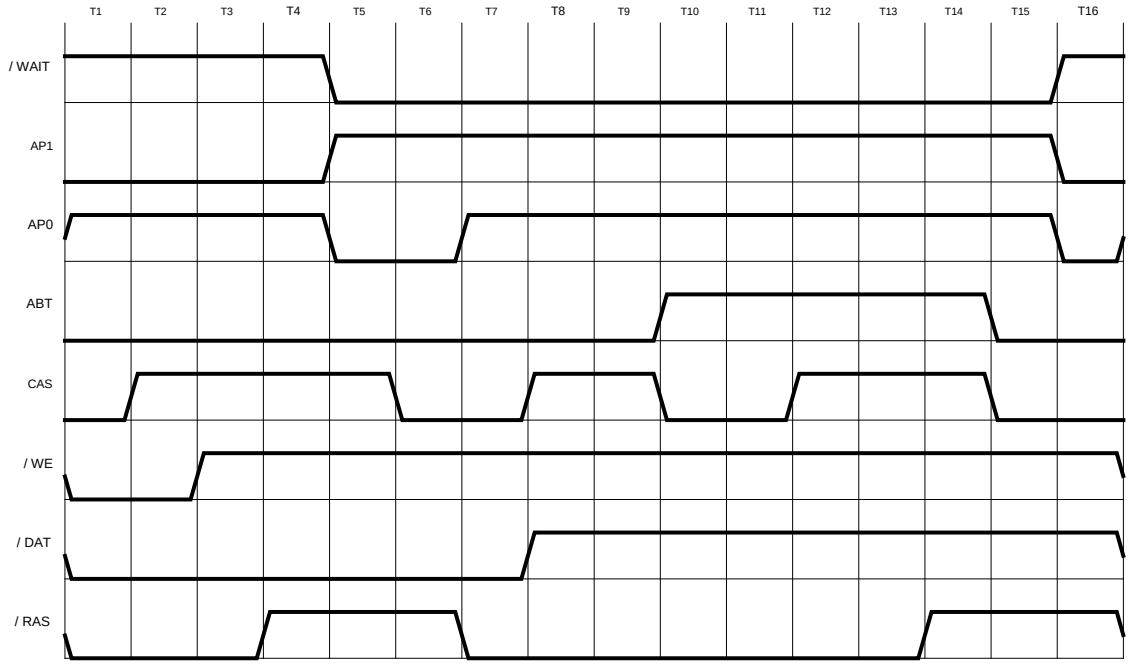


Fig. 4: Timing diagram D18 K155RE3 «M»

2.11 firmware dumps K155RE3, K554RT4

CODE TEXT FOR VILNUS VARIANT V.1989 SINCLAIR ** 155RE3 (M)

May 15 B5 B2 A2 35 26 76 76 6E 6E 7E 7E FE E6 E1 May 15 B5 B2 A2 35
26 76 76 6E 6E 7E 7E FE E6 E1 155RE3 (D)

B4 B5 B6 FF BB CB DB FF 3B 4B 5B FF 74 75 76 FF 8B 9B AB FF 8B 9B AB
FF 0B 1B 2B FF 4B 5B 6B FF 554RT4 (C)

0 1 2 3 4 5 6 7 8 9 00 ABCDEF
5 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 10
4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 20
4 5 5 5 5 5 5 5 5 7 7 7 3 3 3 3 30
7 7 7 7 7 7 7 7 5 5 5 5 5 5 5 5 40
5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 50
5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 60
5 5 5 5 5 5 5 5 5 7 7 7 3 3 3 3 70
7 7 7 7 7 7 7 7 5 5 5 5 5 5 5 5 80
3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 90
3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 A0
3 3 3 3 3 3 3 3 3 3 3 3 7 7 7 7 B0
3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 C0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 D0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 E0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 F0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 554RT4 (K)

0 1 2 3 4 5 6 7 8 9 00 ABCDEF
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 10
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 20
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 30
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 40
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 50
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 60
4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 70
4 4 4 4 4 4 4 8 8 8 4 4 4 4 4 4 80
4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 90
4 4 4 4 1 0 0 0 0 0 0 0 0 0 0 0 A0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 B0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 C0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 D0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 E0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 F0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 ZQ1 = 16.0MHz

Today, there are several versions of the firmware, perhaps with improved characteristics. V.1989 dumps are listed for historical purposes.

3 Tips for assembly and installation of the PC "Baltika"

3.1 Selection of PCB

To successfully build and run your computer will need to purchase a high-quality printed circuit board. When choosing a PCB should pay special attention to specific defects in printed circuit boards:

- the absence of metallization of holes;
- micro-cracks and stains the printed conductors;

- neprotravlennye sections board between conductors;

- poor quality coating conductors (tinning etc).

3.2 Clearing PCB defects

It is necessary to solder the hole card is not used for installing the components. If the solder does not flow on the opposite side of the board, with board Solder tinned wire on both sides. Armed with a magnifying glass, check fee. Your task: to check the printed conductors and the spaces between them, noting gaps and cracks in the printed conductors, to cut the jumper and neprotravy between conductors, solder space gaps and cracks.

3.3 Method of assembly

Connect + 5V pin and GND board with each other and connect them with a soldering iron body. Install all the diodes, resistors, capacitors, sockets and circuit according to the wiring diagram in Figure 3. Solder all the elements of drawing attention to the key position at the chip, the polarity of the respective capacitors, names conclusions transistors and diodes. Implement the missing electrical connections with a thin insulated wire. If you solder D1-D8 elements, it is advisable to pre-test them.

3.4 Connecting to a TV

Once you have all the elements soldered into the PCB, the upper right corner of the field assembly Collect shaping circuit signals R, G, B (see. Fig. 2).

To connect to the TV signals are used SYN, R, G, B, SOUND. SYN signal through the capacitor is 1 uF immediately fed to the TV video input. The signals R, G, B are connected, depending on the used chroma module. The illustrations (not available in this version, due to the obsolescence of these TV models) are possible options for connecting signals R, G, B. To signal that comes from the module UPCHI TV does not interfere, you must put the switch to lock UPCHI module. To connect to a TV chornobelomu additionally assemble circuit is shown in Figure 5. After you prepare your TV and fee, you can start setting up.

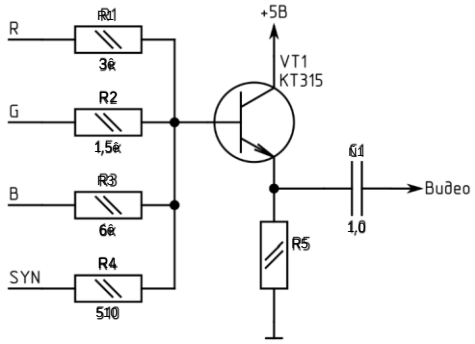


Fig. 5: Connection to a black-and-white television

3.5 First start your computer

Once again, take the wiring diagram and carefully check the correct installation of all chips, diodes and other components, matching their names and denominations schematics and connection diagrams. Thoroughly washed on board, review the pads, solder connections and possible hair occurring during soldering, using a magnifying glass. Eliminate all the detected defects and inconsistencies. Remove the locking pin from the conductor board + 5V and GND.

Connect the power bus with power supply buses via a fuse 2A. Pay particular attention to the polarity of your PC "Baltika" to the power supply. To protect your computer, connect to the + 5V pin and GND zener KS156 or KS815A. Connect a keyboard and a television to your computer.

If you have correctly followed all the recommendations, and all of the installed components on the board are OK, after the power supply to the screen you will see a black square, retractable

vertical stripes. After a moment, the screen will clear and you will see the inscription (intro) «© 1988 BALTIK RUSSIAN» or «© 1982 Sinclair Research Ltd», depending on the version of the system software in ROM D46 and D47. If this does not happen, then you have come close to setting up your PC "Baltika".

3.6 Setting Up Your Computer

First, check the fuse. If the fuse blows, find the short stack on the board, check the polarity of power, damage to the power supply.

For further work you need an oscilloscope with a bandwidth of at least 5 MHz. Connect the oscilloscope to the chassis GND line computer and, if possible, ground it. Setting the easiest way to carry out removing the panels from the ROM D46, D47 and D46 microprocessor. In the absence of these chips on the TV screen to be square with a checkerboard field. In the absence of a square with a checkerboard field, it is first necessary to check the operation of the clock generator D37.6, D37.5, D37.4, frequency dividers D20, D21, D22, D23.1, D23.2. All signals, links to which are provided in the configuration are given in the appendix (see. P. 22). Check up pulses horizontal and vertical sweeps at D27 (10). In their absence, test for resistance R32 D27 (10), the presence of signals D27 (5, 6, 7, 4, 3, 2, 1, 15). In the absence or irregular shape signals D27 (1

Absence or irregular shape of the signal in the presence of all above conditions of a malfunction or faulty chip firmware. In the absence of a signal on the output member do not rush to replace that element, try conductors by cutting the printed circuit board to eliminate the influence of other elements inputs. And only then make a replacement item.

Check the signals R, G, B. In their absence check path forming these signals starting from a memory D1-D8, check the input and output signals to the registers D10, D11, D12, on the multiplexer D19, converts the parallel code register D12 in the serial code . Check signal generating circuit and BORD POINT, multiplexers D30 and D36. In the absence of the timing charts in Appendix 1 for some conclusions chips should only make available pulses, as in the application (see. P. 22) shows the signals mainly having a periodic shape. Particular attention should be paid to the signals generated by PROM K155RE3 «M» (D26), since they control the timing of memory accesses.

After appearing on the screen with a square checkerboard field, you can proceed to the next setup step.

Attention! All manipulations with the EC and other work is performed with the power off your computer. This will save you from trouble. Insert the socket or solder the microprocessor Z80.

When you press the Reset button on the screen, vertical lines should appear (see. Fig. 6). By the reset signal the microprocessor reads the zero address of the first instruction code. Since the ROM is not established, and the data bus through resistors 10 kOhm filed +5 volts, then the microprocessor reads #FF code. #FF code - a team of fixed transition to a subroutine address

In 0038 transition team microprocessor writes the contents of the program counter (# 0038 +
0001 = # 0039) in the stack, the stack is reduced by two. The microprocessor reads again #FF command code at # 0038, again there is a write command the contents of the counter into the stack, etc. As a result, all memory registers code # 0039 and the screen takes the form as shown in Figure 6. If on pressing the button Reset screen does not become as shown in Figure 6, you must:

- press and hold the Reset button, the oscilloscope, check the condition of tires address, data and control Z80 microprocessor,
- data bus - a logical unit of all findings,
- bus address and control - 1-2 Volt (leakage TTL inputs).

It is necessary to define the circuits with tires + 5V and GND. View the status of these tires in different parts of the board.

Z80 signals for proper operation at the terminals must match the information in the table 3.

The absence of any of these signals may cause a malfunction of the microprocessor.

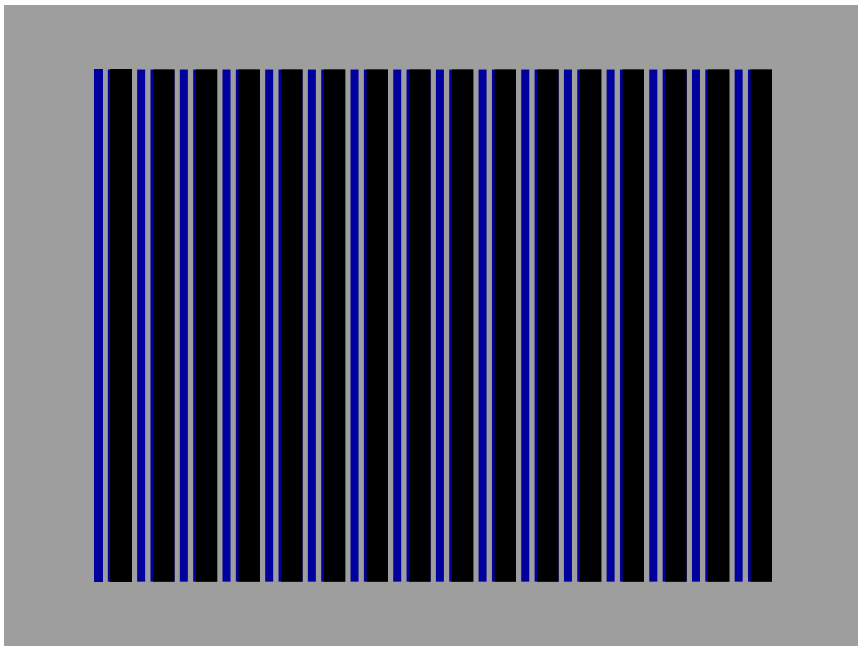


Fig. 6: Screen when filling the code # 0039

Table 3: Signals at the Z80 CPU conclusions

Output Signal Status			Comment
26	/ RESET L;	H	while pressing the Reset; when pressed the Reset button
17	/ NMI	H	constantly
25	/ BUSRQ H		constantly
6	CLK	meander	clock frequency D37 (3)
16	/ INT	L; short negative pulses with a period of 20 milliseconds	in the absence of a ROM; Upon successful completion of the memory test
24	/ WAIT pulses with period	1 microsecond	D26 (1) (see. Fig. 4)

Once you have vertical stripes on the TV screen go to the computer with the commissioning of the ROM.

If the inserted ROM image does not appear on the screen, check if there are sampling pulses ROM D46 (20, 22) and D47 (20, 22). In their absence check scheme for generating these signals.

If the screen you black rectangle with vanishing or fixed red vertical stripes, such an image is formed with a stub RAM test, by reason of a fault or malfunction of IC K565RU5 D13 (provided if D13 (1) and D13 (19) pulses are present).

If you do not have an oscilloscope, you can check the operation of the processing unit using an ordinary tester. To do this, you must collect a diagram is shown in Figure 7. This scheme allows you to organize incremental mode Z80 microprocessor. As a result, you may see many signals in the static mode. This scheme can be assembled on a circuit board, making connections insulated wires. To connect it to the motherboard is necessary to cut the bond connecting D26 (1) and D48 (24), and in this regard, the gap soldered circuit board terminals.

After connecting this board, when you press the Reset button, the microprocessor selects the zero address (# 0000), the first byte of the reset command routines. The next byte is selected at # 0001 by pressing the "Step" button, etc.

Table 4 below shows the bytes on the data bus and the address at which the microprocessor selects the reset command when the subroutine.

Table 4: Information on the tires during the reset subroutine

Address 16 hex	These 16-ary	notes
0000	F3	BORDER becomes white; B is recorded in the port number # 07
0001	AF	
0002	11	
0003	FF	
0004	FF	
0005	C3	
0006	CB	
0007	11	
11CB	47	
11CC	3E	
11CD	07	
11CE	D3	
11CF	FE	
11D0	3E 3F	all memory registers value # 02 (red stripes on the TV screen)
11D1	ED	
11D2	47	
11D3	00	
11D4	00	
11D5	00	
11D6	00	
11D7	00	
11D8	00	
11D9	62	
11DA	6B	
11DB	36	
11DC	02	
11DD	20	
11DE	2B	
11DF	BC	
11E0	FA	
11E1	A7	
11E2		
11E3	ED	Memory test (retractable vertical stripes)
11E4	52	
11E5	19	
11E6	23	
11E7	30	
11E8	06	
11E9	35	
11EA	28	
11EB	03	
11ED	35	
11ED	28	
11EE	F3	
11EF	28	
11F0	D9	recording system variable PRAMT (physical address of the last memory cell)
11F1	ED	
11F2	43	
11F3	B4	
11F4	5C	

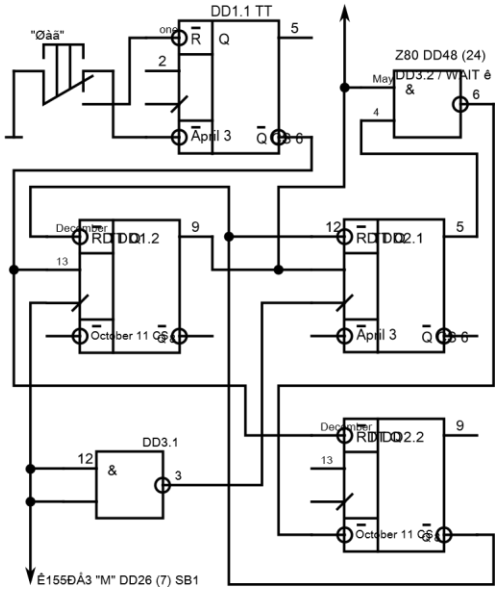


Fig. 7: Scheme for stepping mode CPU Z80

Consider the example of debugging:

1. Press the Reset button:

   (A) at pin D48 (24) a logical zero (/ WAIT microprocessor is able to "expectation"); (B) on the address

   bus # 0000;

   (C) to D47 (20), D46 (20) a logical zero. If the zero level is not present, see the chain formation of this signal D33.2, D37.1, D33.3, D38.1; (D) to D47 (22) a logical

   zero;

   (E) in the presence of zero levels at D47 (20, 22) is present on the data bus # F3 (see. Table. 4).

2. Press the "Step":

   (A) at pin D48 (24) a logical zero; (B) on the address bus #

   0001;

   (C) to D47 (20), D46 (20) a logical zero; (D) to D47 (22) a logical

   zero; (E) bus #AF data (see. Table. 4).

3. Press the "Step":

   (A) the method of procedure 2a; (B) on the address bus

   # 0002; (C) similarly to item 2c; (D) similarly to item 2d; (E)

   on the data bus # 11 (see. Table. 4).

Usually it is sufficient to make 5-6 steps to verify that the sample from the ROM, a data bus, address bus, etc.

At discrepancy information the reduced signal values above, we can use the method of cutting a conductor in order to identify the influence of chips to each other. If after 5-6 steps All the above signals correspond, the set-up of the processor can be considered complete.

Unfortunately signals the memory management can not be viewed in a static, so in this case it is best to use the test [one] ROM.

[one] Test ROM or "test-ROM" - a separate ROM chip with a computer testing program that replaces the D46 and D47, temporarily connectable during debugging in place D47.

When setting up the computer follow the supply voltage. Should try to start a computer and when a higher supply voltage to 5.3 volts.

If you finally got the wallpaper on your TV screen, check the keyboard operation. If the computer does not respond by pressing a key, check if there are short negative pulses with a period of about 20 milliseconds per input / INT D48 (16). In their absence check circuit set and reset latch D39.2. Then, check the presence of short negative pulses with a period of approximately 20 milliseconds D35 (4). If none of the buttons is not closed, then at D35 (1, 6, 10, 13, 15) must present a logical zero. If at least one input and a logic unit is correctly connected keyboard, the device must be replaced.

After adjusting the keyboard is necessary to proceed with the verification of input-output ports.

3.7 Port input from tape

Connect the cassette recorder to your computer. Set the tape cassette into the ZX Spectrum format. Type the following command:

```
LOAD ""
```

Start typed commands to perform the ENTER key and turn on the recorder for playback. When the start-tone signal to the screen output curb horizontal red and blue stripes, smoothly moving vertically. By varying the width of the bands check signal from the tape. When loading a start-signal at the output D45 of the comparator formed TTL level square wave. Loading program after the start signal will display a message:

```
Program: NAME
```

Ports BORDER, TO (yield on the tape) and SO (sound output) implemented on the D42 register. Check the operation of the port and the computer BORDER video block, performing operators BORDER, INK, PAPER BASIC language with different values of 0 to 7, for example:

```
BORDER 1
PAPER 2 INK
7
```

Check the audio channel by performing:

```
BEEP 5,10
```

The computer displays the beep duration of 5 seconds. Check the output port on the recorder,
performing the following command:

```
SAVE ¨NAME¨CODE 0,16384
```

The display for the preparation of the tape will be displayed, press any key meaningful. The screen displays the start-signal bandwidth and output to tape begins ROM contents of your computer. Rewind the tape to the start made by the recording and check the recording by using the command:

```
VERIFY ""CODE 0
```

3.8 Connection and check Kempston joystick

To connect Kempston joystick port used 5 inputs A D44. Conclusions port A D44 (1, 2, 3, 4, 37, 38, 39, 40) through eight resistors 10K connect the GND line. Print the connector under the joystick, and D44 are wired in accordance with the conclusions of the appointment of the connector pins.

D44 (40) - Fire (Key Fire);

D44 (1) - up (Key Up);

D44 (2) - down (Key Down);

D44 (3) - left (Key Left);

D44 (4) - to the right (Key Right);

In general joystick connector conclusion output +5 volts through resistor 0,68-1 ohms. Plug the joystick, the program line by line, type:

```
10 LET A = IN 31; 20 30
PRINT A PAUSE CLS 5
40 50 GO TO 10
```

Run the program to perform a RUN command (press ENTER). On the TV screen, you should see the number 0. Inspect all joystick functions, performing actions and comparing the result to the points of the screen:

1. Push the joystick handle to the right. You should see the number 1.
2. Push the handle to the left joystick. You should see a number 2.
3. Push down the joystick handle. You should see the number 4.
4. Push the joystick handle upwards. You should see the number 8.
5. Press the button on the joystick. You should see the number 16.

If the values correspond to the numbers given above, the joystick port and a slot for him properly connected, the joystick works.

3.9 Some of the situations that arise when setting up your computer

1. With the computer on the TV screen appear dashes, dots, or lost part of the symbol. This is due to incomplete regeneration RAM. In this case it is necessary to tighten experimentally fronts signal AP0 D26 (3) and / RAS D26 (9), connecting the capacitors 10-300 pF capacitance therebetween and a line GND.

2. When using K556RT4 «C» chipset old issue has often been on the curb and sometimes on the visible side of the screen there are dark strips (and on your computer are not affected). In this case it is necessary either to replace K556RT4 «C» (D27), or by means of capacitors, tightening the edges of the signals POINT D36 (14), D30 (14) and BORD D36 (2), D30 (2), to achieve their reduction or disappearance.

3. On the TV screen in each familiarity thin strips in one pixel. This occurs due to a malfunction of one of the bits of the register D12 or an open connection between the outlet of the discharge and the corresponding input D19.

4. Not displayed system software saver. Checking with the test ROM is successful (RAM properly). Sequentially after resetting: black square, retractable vertical stripes, the screen goes white, but the image does not appear. Check signal conditioning circuit D39.2 reset trigger. Due to the presence on the microprocessor input / INT zero level occurs at the loop processing of interrupts.

5. Press once on the key on the keyboard, two or more characters are entered. This is due to spurious peaks at pin D28 (12), which during the time interval of 20 milliseconds is set 2-3 times D39.2 trigger. As a result, it also disrupted the operator PAUSE BASIC language. It is necessary to flip-flop set input D39.2 (11) to signal to D23.2 (13), thus breaking the old connection c D28 (12). This refinement also sets the time of formation of an interrupt to a position more compatible with the original ZX Spectrum.

4 Improvements

4.1 Stretching the paper area on the TV screen

Because of the use of the quartz resonator in the Baltic Sea to 16 MHz, the area sizes of paper (Paper) is smaller and the size field border (Border) right and left at the television screen than in other embodiments, a quartz resonator of 14 MHz. Display graphics slightly compressed horizontally.

To modify your PC "Baltika" at the frequency of 14 MHz is necessary:

1. Replace the quartz resonator 14 MHz
2. Replace D27 K556RT4 «C» chip. Firmware K556RT4 «C» for 14MHz is shown below.
3. Between the terminal D27 (9) and the + 5V line connected pullup resistor of 1 k.
4. Connect the terminals D27 (9) and D21 (9) after disconnecting from the last line of + 5V.

556RT4 (C)

0 1 2 3 4 5 6 7 8 9 00 ABCDEF
DCCCCCCCCCCCCCCC 10
CCCCCCCCCCCCCCCC 20
CDDDDDFFFBBBBFFF 30
FFFDDDDD 5 DDDDDDD 40
DDDDDDDDDDDDDDDD 50
DDDDDDDDDDDDDDDD 60
DDDDDDFFFBBBBFFF 70
FFFDDDDD 5 DDDDDDD 80
BBBBBBBBBBBBBBBB 90
BBBBBBBBBBBBBBBB A0
BBBBBBBBBFFFFBBB B0
BBBBBBBB 3 BBBBBBB C0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 D0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 E0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 F0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 ZQ1 = 14MHz

4.2 Correct formation signal / INT

To increase the stability of the program it is necessary to change the method of formation of the recession signal / INT. The circuit PC "Baltic" D39.2 reset trigger signals is carried out using / M1 and / IORQ, which does not give stable duration / INT. Figure 8 shows the change of scheme. The duration of the signal / INT should be 7-9 microseconds.

Evidence of properly chosen circuit is the fact that the prevalence of test hardware ZX Spectrum on your computer right to the end of the keyboard will pass the test. Usually idle Samantha Fox program will run smoothly.

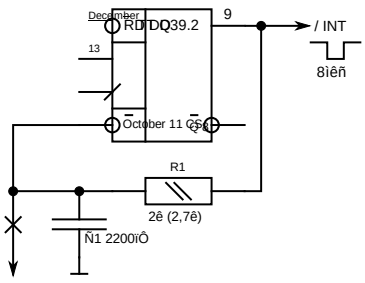


Fig. 8: Diagram correct the signal / INT

About 5 interchangeability of components

Chips K555 series, with the exception of D14-D17, you can replace the same series K155, K1533 and K1531.

K561 series chips can be replaced by similar series K564 and K1561. K565RU5 memory chips can be placed with any suffix "B", "B", "G", "D", with the exception of "D1" and "D2".

K555IR27 chip can be replaced by K555IR23.
Chip D13 K555AP6 a small completions board can be replaced by K580VA87. Multiplexers K555KP12 except D14-D17, can be replaced by K155KP2. If you put the D14-D17 K155KP2, you must remove the signal delay element / RAS D25.2. Chip K555KP15 D19 can be replaced by K155KP7. Counters can be replaced by K555IE10 K555IE18.

Instead of the ROM can be put K556RT4 K556RT11. In this case, no need to put a pull-up resistance.

Instead D37 K531LN1 better to put K1533LN1. Power consumption in her 5-6 times less than that of K531LN1.

Instead D45 K554SA3 can put K521SA3. Chip 2764 can be replaced by K573RF4.
Instead stabistorov KS119A can put an ordinary LED AL307 or two series-connected diodes KD522.

6 Applications

6.1 Annex 1. Waveforms

All measurements are made on the oscilloscope S1-65.

number of chips	Pin number	Signal Name	Waveform number
D1-D8	4	-	1
	15	-	2
D9	1	-	3
	2	-	4
	4		4
	5		5
	8		6
	9		7
	10		3
	11		8
	13		8
D10	11	TT	9
D11	11	/ABT	10
D12	11	TT	9
D14	2	-	11
	4	-	12
	12	-	13
	14	-	14
D15	2	-	11
	3	-	15
	4	-	16
	12	-	17
	13	-	6
	14	-	14
D16	2	-	11
	3	-	15
	4	-	19
	12	-	20
	13	-	21
	14	-	14
D17	2	-	11
	12	-	22
D18	3	-	3
	4	-	6
	5	-	15
	6	-	21
	7	-	18
	10	-	23

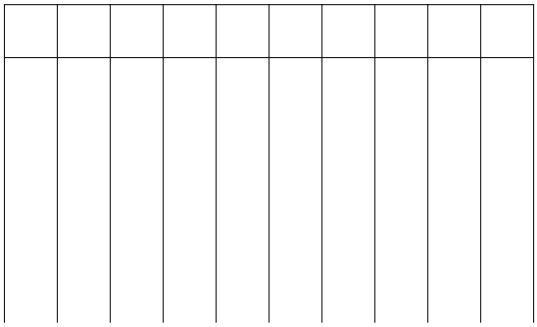
	11	-	24
	14	-	10
D19	9	1M	25
	10	2M	26
	11	4M	27
D20	2	-	28
	11	-	25
	12	-	26
	13	-	27
	14	-	29
	15	-	30
D21	2	-	28
	7	-	30
	11	-	16
	12	-	17

Chip number	Pin number	Signal Name	Waveform number
	13	-	12
	14	-	13
	15	-	31
D22	2	-	28
	7	-	30
	10	-	31
	11	-	5
	12	-	4
	13	-	32
	14	-	20
	15	-	33
D23	1	-	33
	3	-	7
	4	-	19
	5	-	22
	7	-	34
	11	-	23
	12	-	24
	13	-	46
	15	-	34
D25	5	/RAS	35
	6	-	1
	8	-	2
	10	-	37
	11	-	36

	12	CAS	36
D26	1	/WAIT	38
	2	AP1	11
	3	AP0	14
	4	/ABT	10
	5	CAS	36
	6	/WRE	39
	7	/DAT	40
	9	/RAS	35
	10	8M	29
	11	4M	27
	12	2M	26
	13	1M	25
D27	1	-	45
	2	-	32
	3	-	23
	4	-	16
	5	-	13
	6	-	12
	7	-	17
	10	SYN	41, 42
	11	-	43
	12	-	8
	15	-	44
D28	1	-	24
	2	-	23
	4	-	22
	5	-	5
	6	-	7
	7	-	19
	9	-	44
	10	-	45
	15	-	46
D31	1	-	30

Chip number	Pin number	Signal Name	Waveform number
	3	-	9
D32	5	-	40
	11	-	47
D33	2	-	39
D34	1	-	48
	11	-	49

D35	4	-	49
D37	5	-	27
	6	-	51
	8	-	28
	9	-	50
	10	-	50
D38	4	-	48
	13	-	43
D39	9	-	52
	10	-	47
	11	-	34
D48	6	/CLK	51
	24	/WAIT	38



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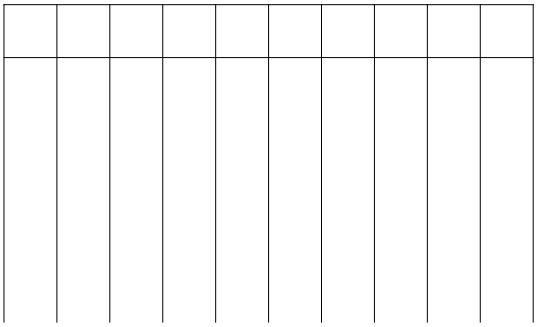

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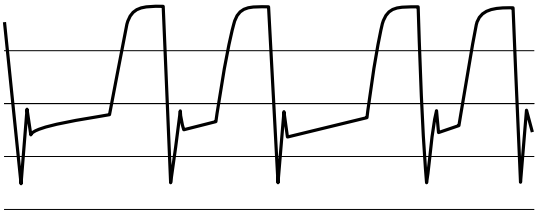

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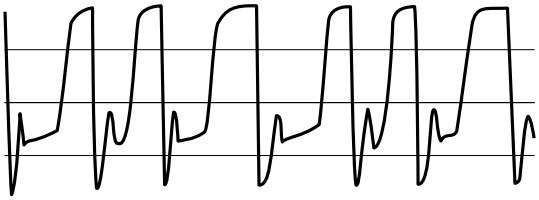

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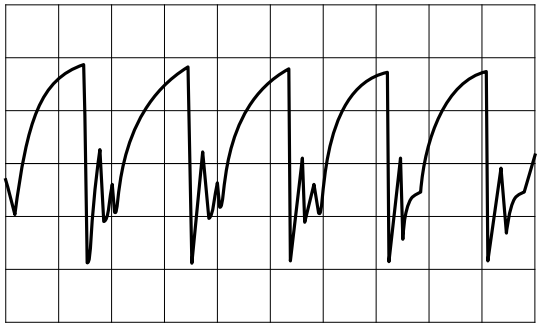

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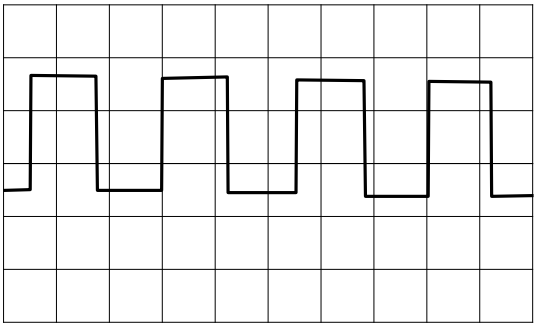

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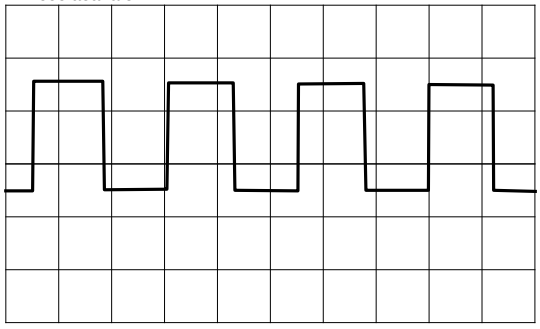

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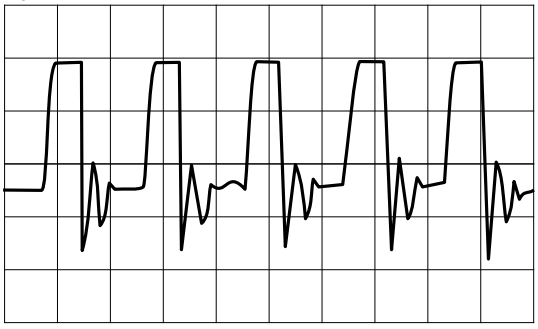

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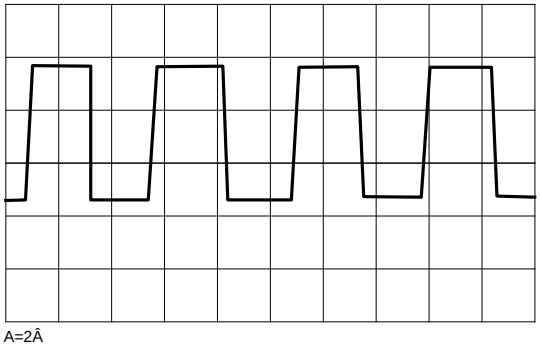

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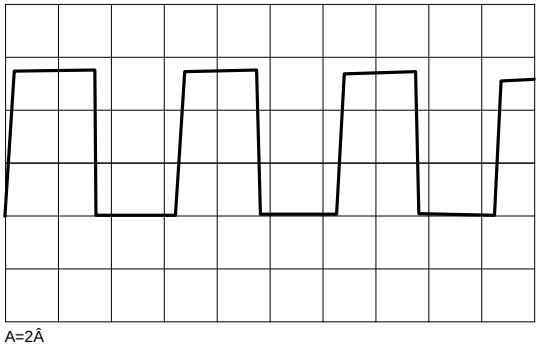

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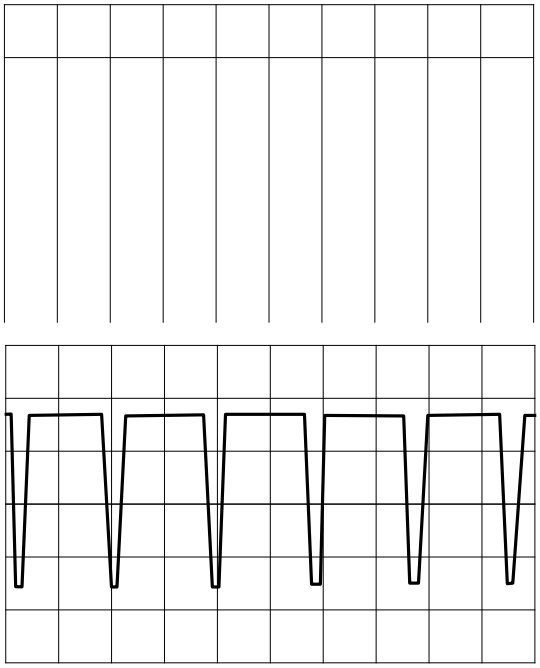

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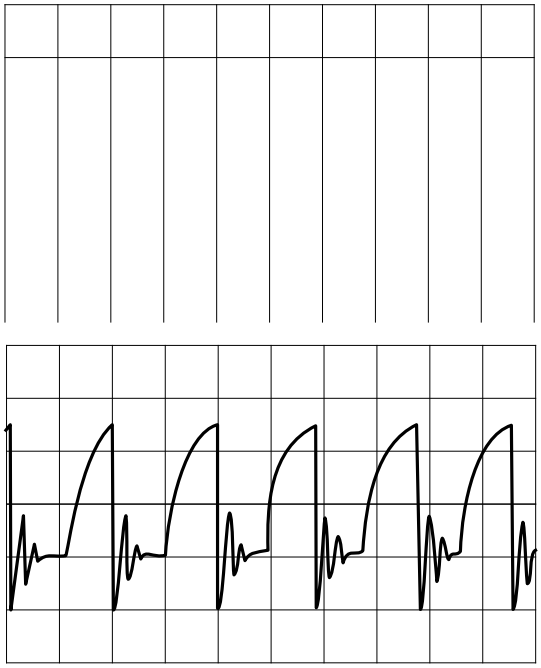

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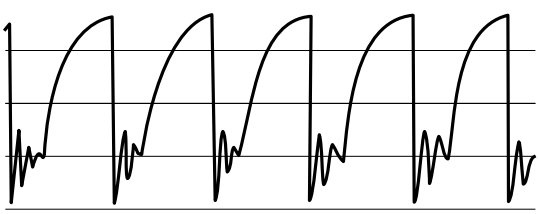

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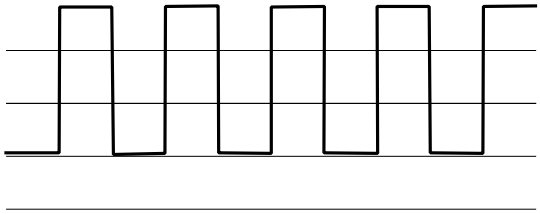

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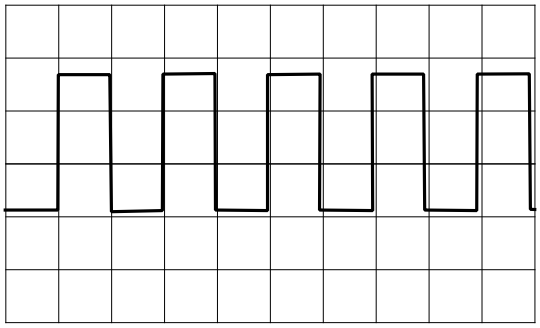

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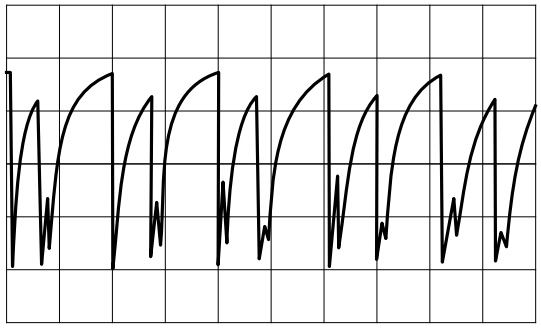

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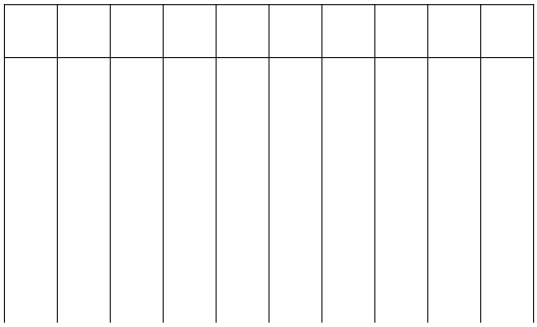
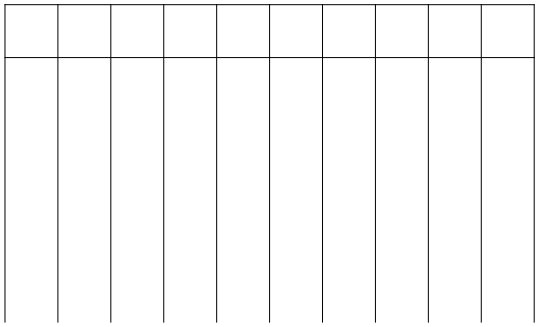
A=2Â





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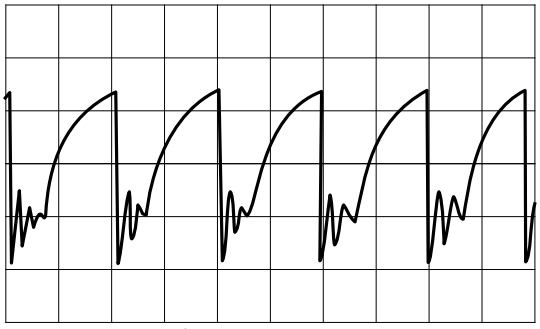

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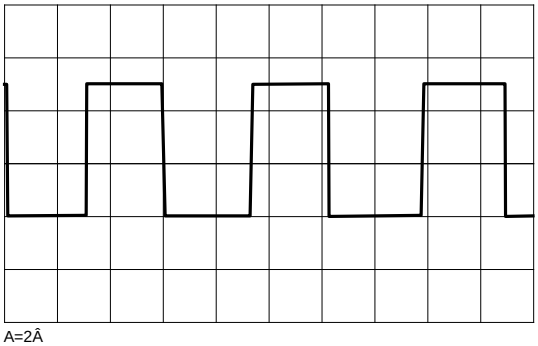

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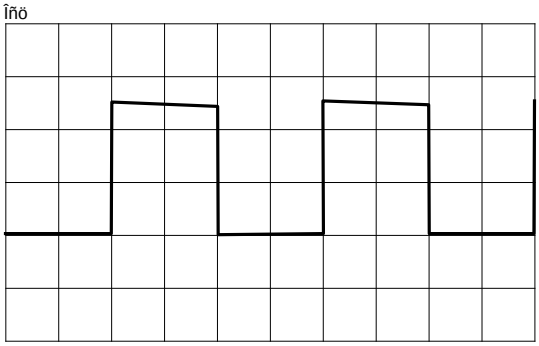

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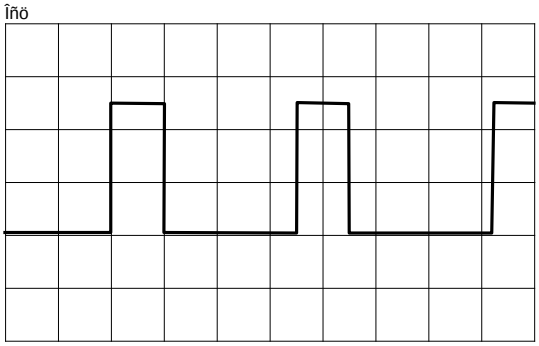

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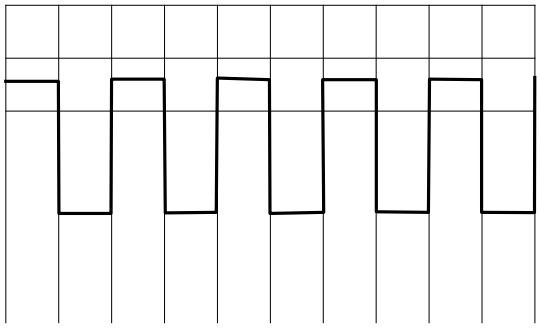
èëëîãðàììà 20



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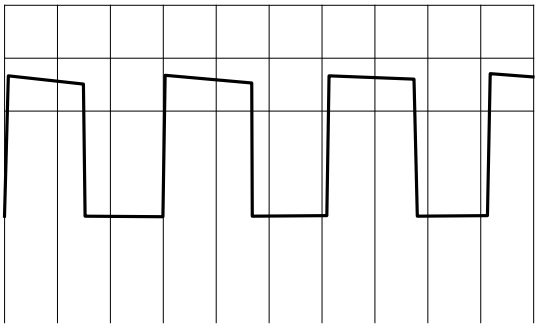

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èëëîãðàììà 22

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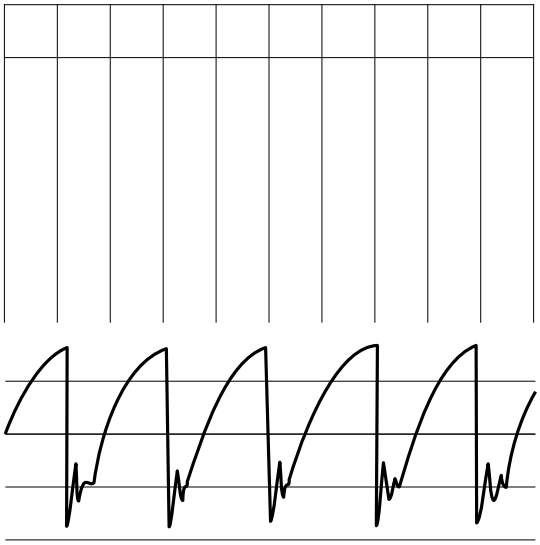

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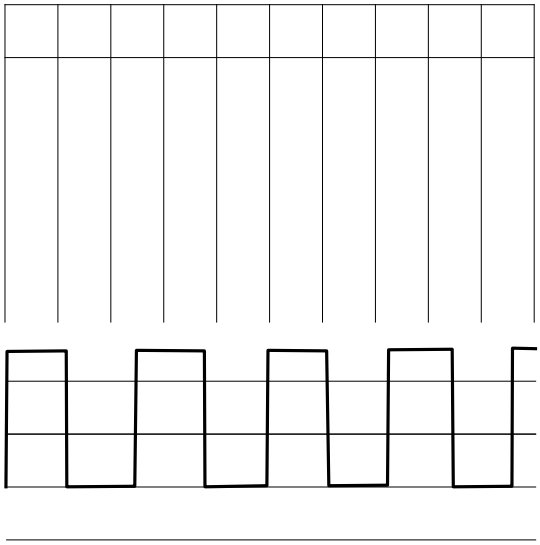

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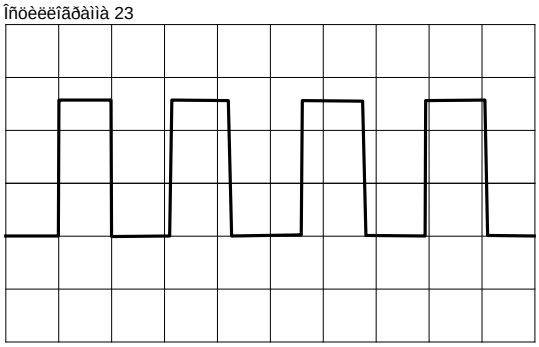
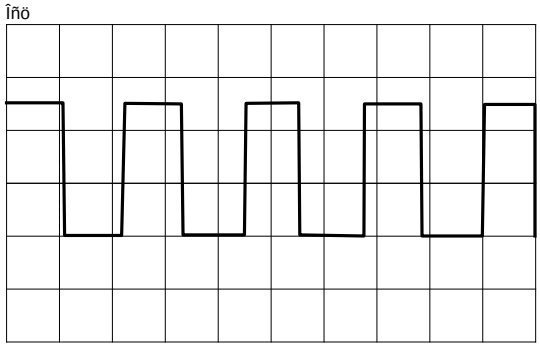


A=2Â

Îñö

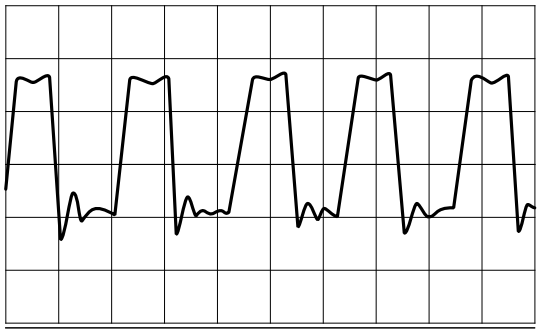


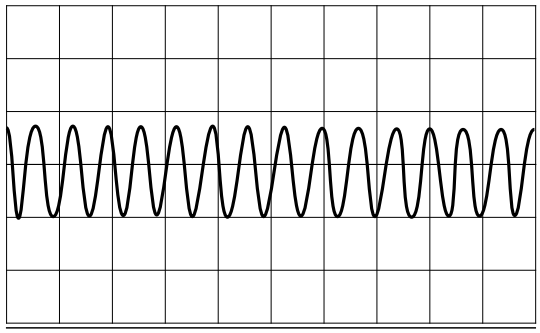
A=2Â

èëëîãðàììà 25

A=2Â T=0,5 ìêñåê.

A=2Â T=0,2 ìêñåê.





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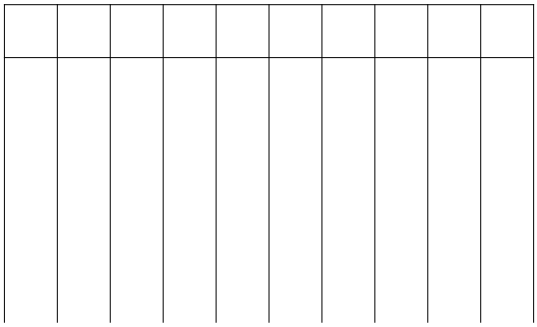

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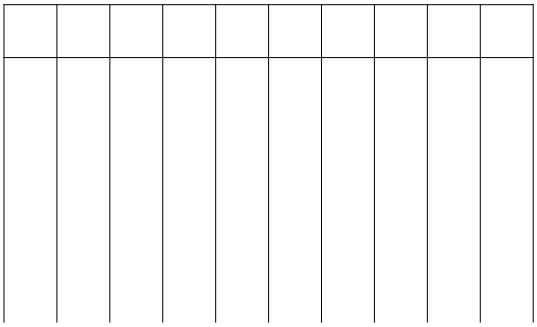

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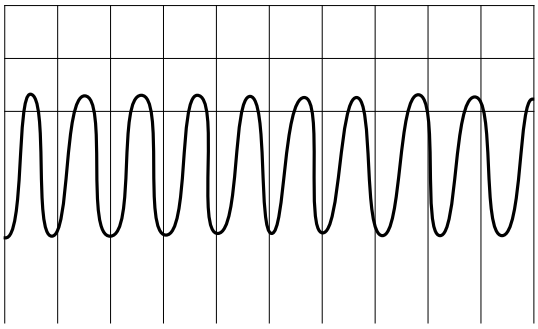
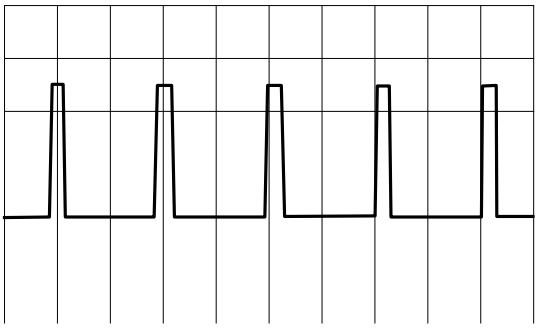


A=2Â T=0,1 ìêñåê.

èëëîãðàììà 30



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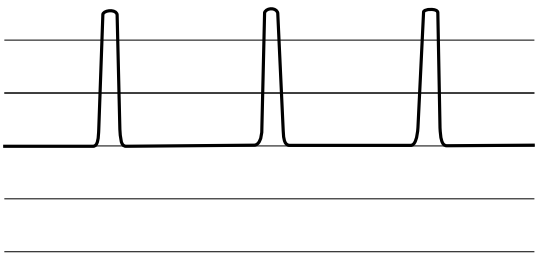

A=2Â

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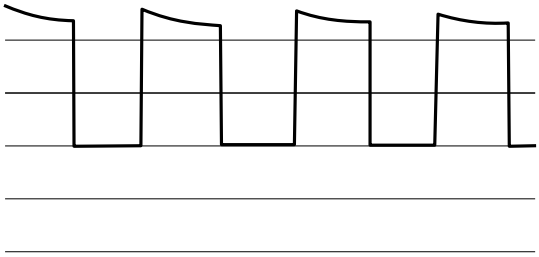

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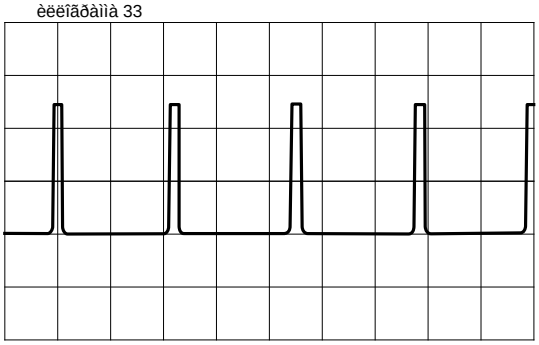

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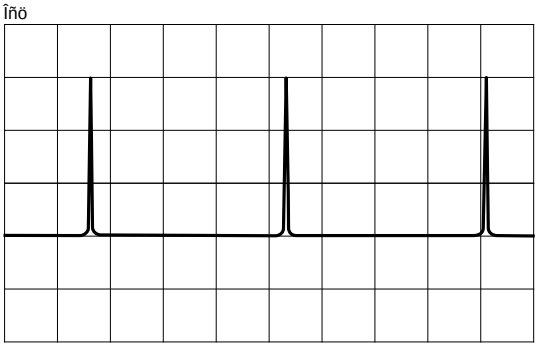
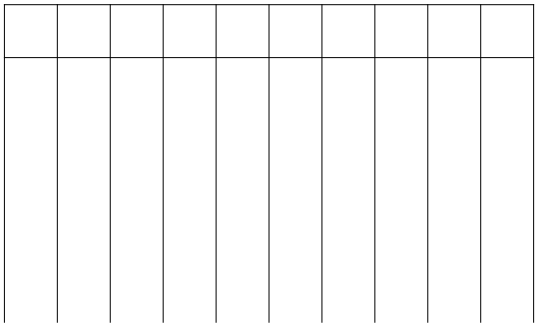
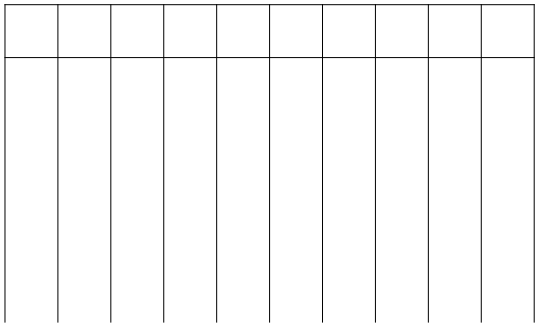


A=2Â

A=2Â





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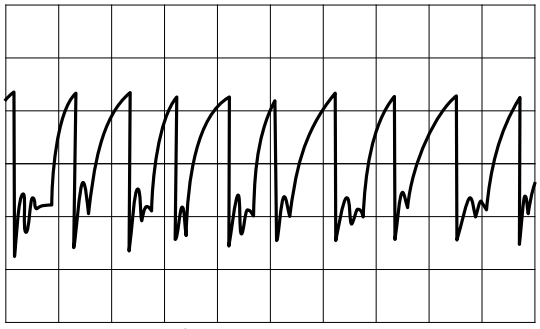

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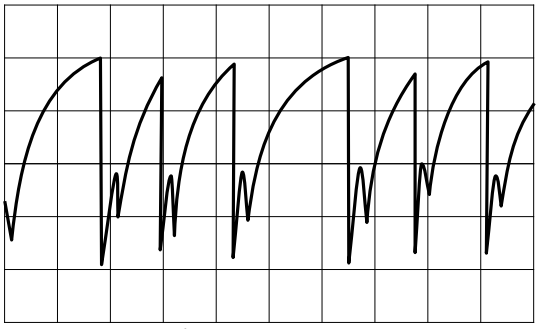

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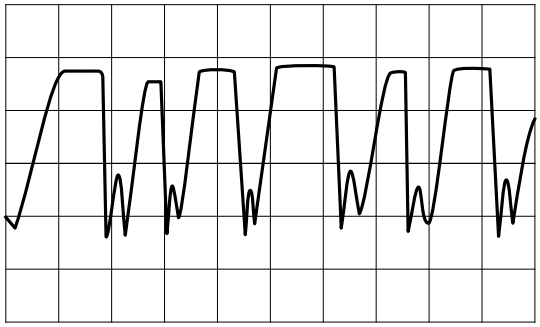

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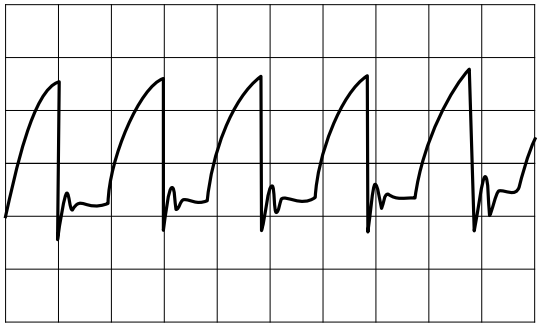

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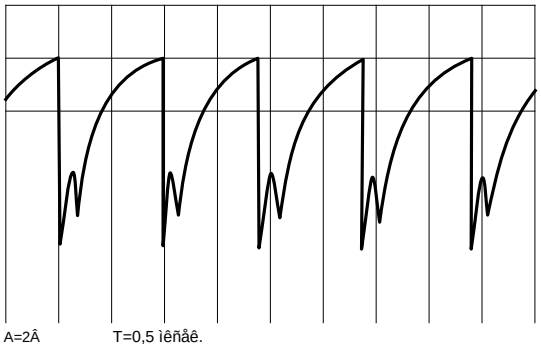

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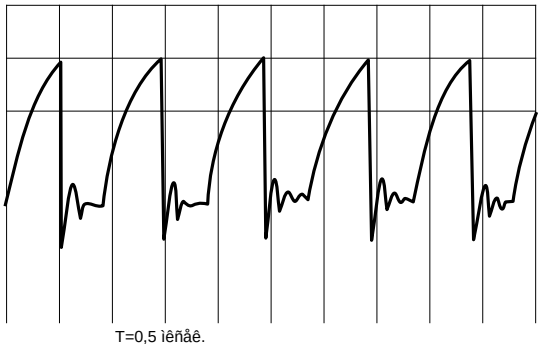
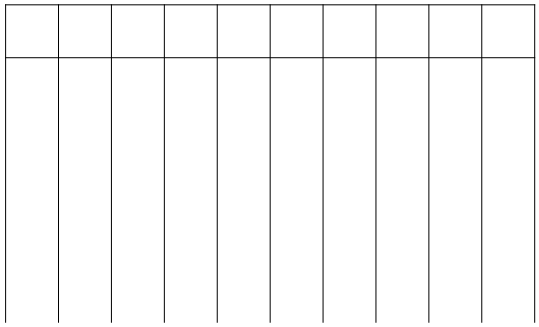


T=0,5 ìêñåê.

A=2Â



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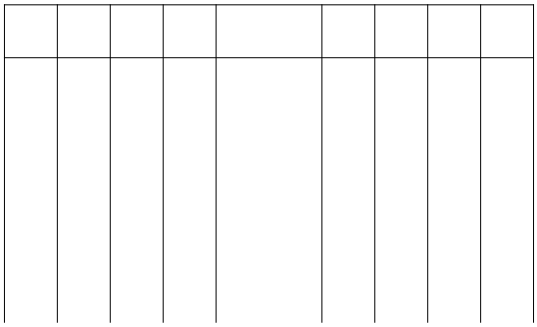

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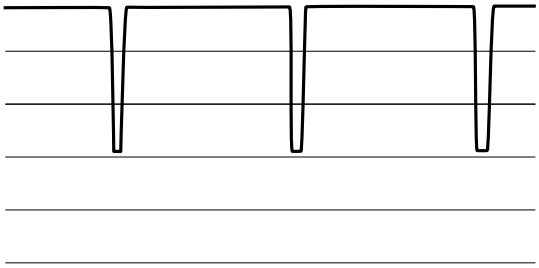

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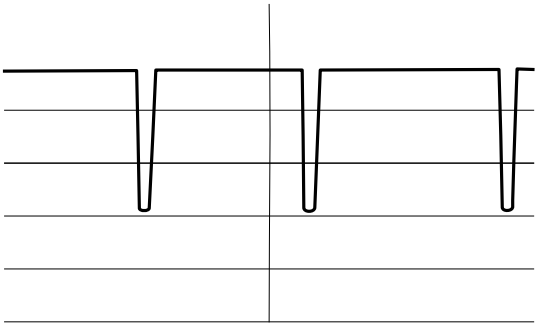

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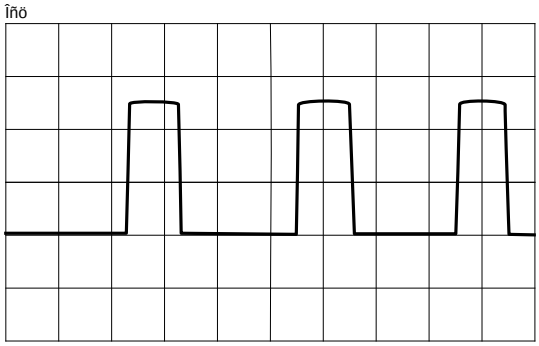

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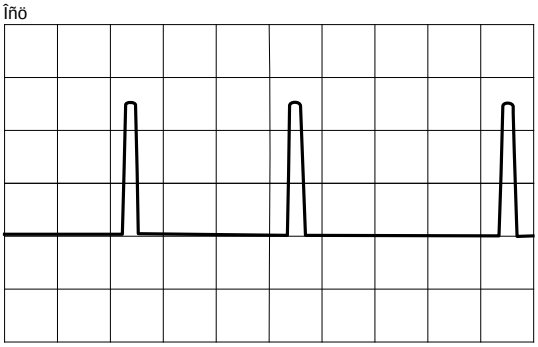

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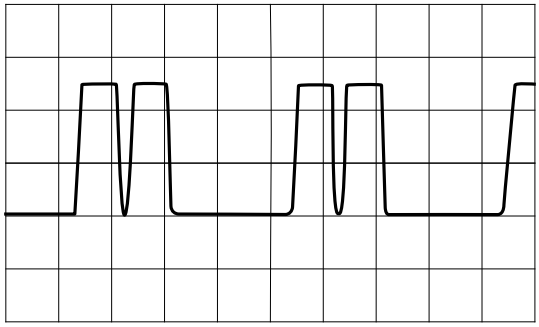
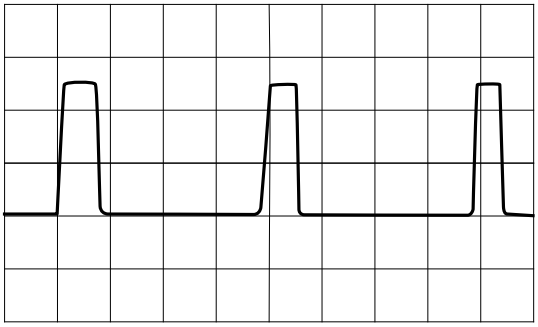


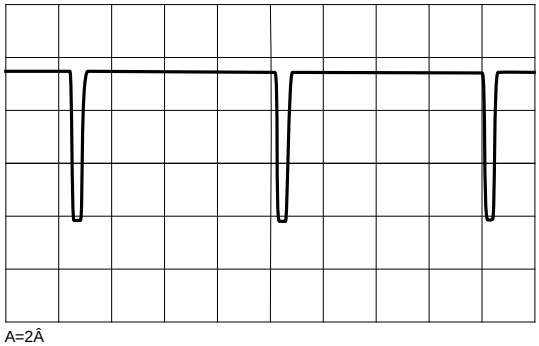
A=2Â

Îñö



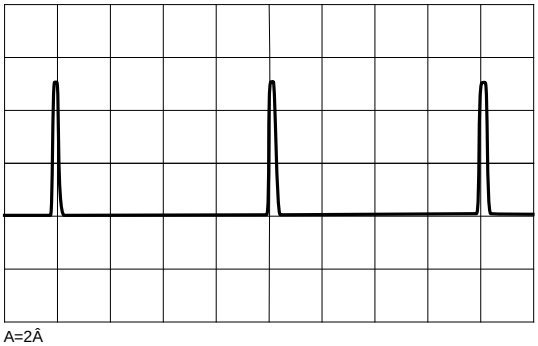
A=2Â

Îñö



A=2Â

Îñö



A=2Â

6.2

Appendix 2. Programmable parallel interface K580VB55

Chip K580VB55 is a programmable input-output device for parallel information. It is used as a general-purpose input-output element that mates various types of peripheral devices. The symbolic graphic designation of the microcircuit is shown in Figure 9, and the pin assignment in table 7.

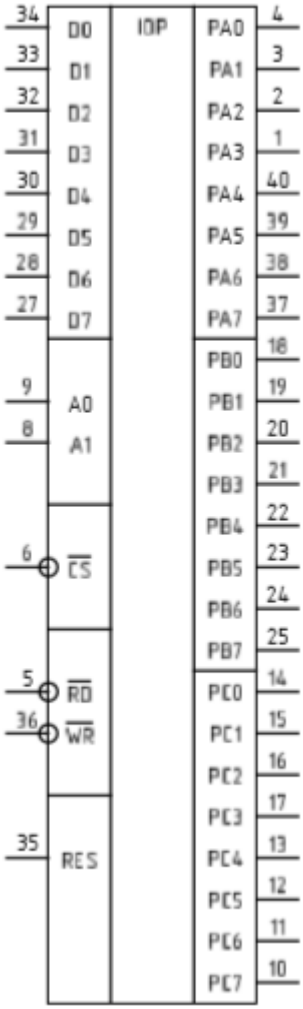


Fig. 9: Conventional graphic designation of IP K580VB55Ta

Fig. 7: Pin Assignment IS K580VV55 Pin Number

Обозначение Наиме	ювание 27-34	
	D0-D7	Канал данных
9, 8	A0, A1	Адрес канала
6	/CS	Выбор устройства
5	/RD	Чтение
36	/WR	Запись
35	RES	Сброс
4-1, 40-37	PA0-PA7	Канал PA
18-25	PB0-PB7	Канал PB
14-17, 13-10	PC0-PC7	Канал PC
7	GND	Общий
26	Vcc	Питание

Information is exchanged between the system data bus and the chip through an eight-bit bi-directional three-stable data channel D. For communication with peripheral devices, 24 I / O lines are grouped into two independent eight-bit channels PA and PB and two four-bit PC channels

The microcircuit can function in three main modes. Modes 0, 1, 2. Connecting a chip in a Baltika computer without any alterations allows you to work in mode 0, so we will consider this mode in more detail. This mode provides the possibility of synchronous program-controlled data transmission through two independent eight-bit channels PA and PB and two four-bit PC channels. The choice of the appropriate channel and the direction of information transmission through the channel is determined by the signals A0, A1 and the signals / RD, / WR and / CS (see table.

8). Table 8: K580BB55 control signals

entrances					Information transfer direction
A1	A0	/RD	/WR	/CS	
Operation in water (reading)					
0	0	0	1	0	PA → data channel
0	1	0	1	0	PB → data channel
1	0	0	1	0	PC → data channel
Operation of the radio (recording)					
0	0	1	0	0	data channel → PA
0	1	1	0	0	data channel → PB
1	0	1	0	0	data channel → PC
1	1	1	0	0	data channel → РУС
Lock operations					
X	X	X	X	1	data channel → third state
1	1	0	1	0	prohibited combination

X - input state doesn’t

The operation mode of each channel is determined by the contents of the control word register (RUS). The format of the RUS is described in table 9.

When a RESET signal is applied to the RES input, the RUS is set to a state in which all channels are set to work in mode 0 to enter information.

The mode of operation of the channels can be changed both at the beginning and during the execution of the program, which allows serving various peripheral devices. Below is the control word format that defines the mode of operation of the channels.

Table 9: Control Word Format

Nazn Bits	Value D0
D0	bits 0-3 channel PC 0 → output 1 → input
D1	channel PB. 0 → output 1 → input
D3	bits 4-7 of the PC channel. 0 → output 1 → input
D4	PA channel. 0 → output 1 → input
D6, D5	operating mode of PA and bits 4-7 PC. 00 → mode 0 01 → mode 1 1X → mode 2
D7	equal to 1[2]

X - the state of the bit doesn't matter

2 Bit 7 RUS - "Control Flag". 0 → operation with bits (not described here), 1 → mode selection.

6.3 Appendix 3. List of components

Designation	Description	Denomination	Quantiy	Packaging
C1	Ceramic Capacitor	300 pF	1	
C2 C4	Capacitor niobium, tantalum, electrolytic	4,7 microfarad	2	
C3	Ceramic Capacitor	1 microfarad	1	
D1 D2 D3 D4 D5 D6 D7 D8	IMS. 64Kbit Dynamic RAM	К565РУ5	8	DIP
D9	IMS. Four buffer elements with three output states	К555ЛП8	1	DIP
D10 D11 D12 D42 ИМС. Pe	eight-bit histogram with recording resolution	К555ИР27	4	DIP
D13	IMS. Eight-channel bi-directional shaper with three states at the output	К555АП6	1	DIP
D14 D15 D16 D17 D30 D36	IMS. Two-bit, four-channel switch with three stable outputs	К555КП12	6	DIP
D18 D26	IMS. Electrically programmable ROM. 256 bits (32 words x 8 bits)	К155РЕ3	2	DIP
D19	IMS. Eight-input selector-multiplexer with three stable output states	К555КП15	1	DIP
D20 D21 D22	IMS. Binary synchronous four-digit counter	К555ИЕ10	3	DIP
D23 D43	IMS. Two four-digit counters	К561ИЕ10	2	DIP
D24 D29 D38	IMS. The six gates are NOT	К555ЛН1	3	DIP
D25	IMS. Four two-way exclusive OR	К555ЛП5	1	DIP
D27 D28	IMS. Electrically programmable ROM. 1024 bits (256 words * 4 bits)	К556РТ4	2	DIP
D31 D40	IMS. Four logical elements 2I-NOT K555LA3		2	DIP
D32	IMS. Four logical elements 2 OR K555LL1		1	DIP
D33	IMS. Three logical elements 3OR NOT K555LE4		1	DIP
D34	IMS. Double	К555ИД4	1	DIP
D35	decoder-multiplexer 2-4	К561ЛН1	1	DIP
D37	IMS. Six logic elements NOT with blocking and prohibition	К531ЛН1	1	DIP
D39	IMS. The six gates are NOT	К555ТМ2	1	DIP
D41	IMS. Two D-flip-flops	К555ТМ8	1	DIP
D44	IMS. Four D flip-flops with direct and inverse outputs	К580ВВ55А	1	DIP
D45	IMS. Programmable parallel interface	К554СА3	1	DIP
D46 D47	IMS. Voltage comparator	SN2764	2	DIP
D48	IMS. Central Processing Unit Z80A CPU		1	DIP

R1 R2 R44 R46 R48	Resistor MLT-0.125	360 ohm	5	
R3 R4 R5 R6 R7 R8 R9 R10 R11 R28	Resistor MLT-0.125	10 kOhm	10	
R12 R13 R14 R15 R16 R17 R18 R19 R20 R21 R22 R23 R24 R25 R26 R27 R29 R30 R31 R32 R33 R34 R35 R37 R38 R39 R40 R41 R42 R45 R47 R54	Resistor MLT-0.125	1 kOhm	32	

Designation	Description	Denomination	Quantity	Packaging
R36			1	
R43	Resistor MLT-0.125	100 kOhm	1	
R49 R50 R51 R52 R53	Resistor MLT-0.125	1.8 kOhm	5	
R55 R56 R57	Resistor MLT-0.125	7.5 kΩ	3	
R58 R59 R60	Resistor MLT-0.125	5.6 kΩ	3	
VD1 VD2 VD3 VD4 VD5 VD6 VD7 VD8 VD9 VD10 VD12 VD13 VD14	Trimmer Resistor	22 kOhm (?)	13	
VD11	Silicon pulse diode	KD522B	1	
ZQ1	Silicon stator low power, U article = 1.9 V	KS119A	1	HC-49U